REMARKS

In the Final Office Action, the Examiner noted that claims 1-20 are pending in the application and that claims 1-20 are rejected. By this response, claims 1, 11, 14, and 17 are amended. In view of the above amendments and the following discussion, the Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1-8 and 10-20 as being anticipated by Chen (United States patent 6,687,888, issued February 3, 2004). The rejection is respectfully traversed.

More specifically, the Examiner stated that Chen teaches designing an integrated circuit in accordance with timing constraint data to produce a design result. (Final Office Action, p. 6). In support, the Examiner cites a portion of the Chen background, which discloses the use of static timing analysis the results of which are fed back to a synthesis tool to improve timing. (See Chen, col. 3, lines 49-67). The Examiner further stated that Chen teaches selectively optimizing the integrated circuit to reduce power consumption. (Final Office Action, p. 6). In support, the Examiner cites a portion of the detail description of Chen, which discloses reduction of power consumption by resizing and changing device types. (See Chen, col. 12, lines 46-53). The Examiner concluded that Chen anticipates Applicants' invention recited in claim 1. Applicants respectfully disagree.

First, to anticipate Applicants' claim 1, Chen must disclose each of the elements in claim 1 having the same arrangement of claim 1. See MPEP 2331. The elements of Chen cited by the Examiner, however, do not have the same arrangement of those of Applicants' claim 1. That is, there is no arrangement in Chen where an integrated circuit is designed in accordance with timing constraint data to produce a design result and then selectively optimized to reduce power consumption. Rather, the disclosure in the Chen background is related to static timing analysis only and not with reduction in

power consumption. In the detailed description, Chen discloses that timing and power are optimized simultaneously to produce an optimized design result. (Chen, col. 8, line 30-67; FIG. 3A; col. 9, lines 1-62; FIG. 4; col. 11, line 32 to col. 12, line 19; FIG. 6). The disclosures in the background and detailed description of Chen are separate and are not part of a single method or process. There is no single arrangement in Chen where an integrated circuit is optimized for timing only and then optimized to reduce power consumption, as recited and arranged in Applicants' claim 1.

Second, Applicants have amended claim 1 to further clarify the difference emphasized above between Applicants' invention and Chen, namely, optimizing the integrated circuit for timing to produce a design result and then selectively optimizing for power. Amended claim 1 recites that the integrated circuit is designed using a timing-driven design process to produce a design result optimized for timing performance and not for power consumption. The design result is a complete result optimized for timing only. (Applicants' specification, ¶0016; FIG. 2). Thus, in Applicants' claim 1, an integrated circuit is first designed in conformity with timing constraint data to produce a design result (e.g., a timing-driven process) and then optimized to reduce power consumption (e.g., a power-driven process).

In contrast, Chen teaches a single global optimization process, where the design is simultaneously optimized for both timing and power. Chen does not teach or suggest optimizing a design for timing to produce a result, and then optimizing the design for power. In Chen, any power optimizations are part of the general optimization process for timing and power. Once the circuit design conforms to the general optimization (e.g., the genetic optimization or greedy optimization) and an optimized design result is produced, no further power optimizations are performed.

Accordingly, Chen does not anticipate Applicant's invention recited in claim 1. Claims 11, 14, and 17 each recite features similar to those of claim 1 emphasized above. For the same reasons discussed above, Chen does not anticipate Applicants' invention recited in claims 11, 14, and 17. Finally, claims 2-8, 10, 12-13, 15-16, and 18-20 depend, either directly or indirectly, from claims 1, 11, 14, and 17 and recite additional features therefor. Since Chen does not anticipate Applicants' invention as

recited in claims 1, 11, 14, and 17, dependent claims 2-8, 10, 12-13, 15-16, and 18-20 are also not anticipated and are allowable.

In view of the foregoing, Applicants contend that claims 1-8 and 10-20 are not anticipated by Chen and, as such, fully satisfy the requirements of 35 U.S.C. §102. Accordingly, Applicants respectfully request that the rejection to such claims be withdrawn.

II. Rejection Of Claims Under 35 U.S.C. §103

The Examiner rejected claim 9 as being unpatentable over Chen in view of Dave (United States patent 6,178,542, issued January 23, 2001). The rejection is respectfully traversed.

More specifically, the Examiner noted that Chen does not disclose the feature of the IC having a plurality of logic paths, where the threshold is defined by a percentage of a parameter in the timing constraint data. (Final Office Action, p. 5). The Examiner stated that Dave teaches such a threshold. (Final Office Action, p. 5). The Examiner concluded that it would have been obvious to combine Dave with Chen to arrive at Applicants' invention of claim 9. Applicants respectfully disagree.

Dave generally teaches hardware-software co-synthesis of embedded system architectures using quality of architecture metrics. (See Dave, Abstract). Dave, however, does not teach or suggest designing the integrated circuit in accordance with timing constraint data to produce a design result and then selectively optimizing the integrated circuit to reduce power consumption. Chen also fails to teach such a feature, as discussed above. Since neither Chen nor Dave teach such a feature, no conceivable combination of Chen and Dave render obvious Applicants' invention of claim 1. Therefore, Applicants contend that the invention of claim 9 is patentable over the combination of Chen and Dave and, as such, fully satisfies the requirements of 35 U.S.C. §103. Accordingly, Applicants respectfully request that the rejection of claim 9 be withdrawn.

CONCLUSION

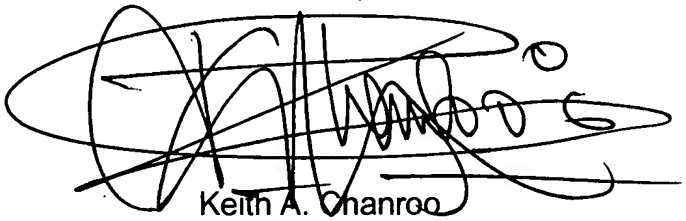
Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of

35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Keith A. Chanroo at (408) 879-7710 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on July 17, 2006 .

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Signature